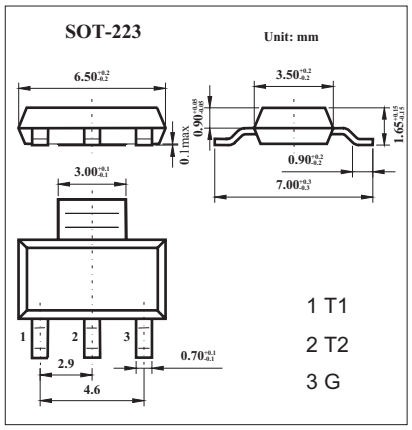
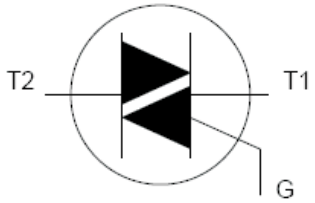
Triacs

BT134W Series

Features

- Repetitive peak off-state voltages :V_{DRM}=500V～800V
- RMS on-state current :$I_{T(RMS)}$=1A
- Non-repetitive peak on-state current :I_{TSM}=10A





Absolute Maximum Ratings Ta = 25℃

Parameter	Symbol	Testconditons	BT134W-500	BT134W-600	BT134W-800	Unit
Repetitive peak off-state voltages	V_{DRM}		500	600	800	V
RMS on-state current	$I_{T(RMS)}$	full sine wave; T_{mb} ≤ 108 ℃	1			A
Non-repetitive peak on-state current	I_{TSM}	full sine wave; Tj = 25℃ prior to surge				
		t = 20 ms	10			A
		t = 16.7 ms	11			A
I^2t for fusing	I^2t	t = 10 ms	0.5			A^2S
Repetitive rate of rise of on-state current after triggering	dI_T/dt	I_{TM} = 1.5 A; IG = 0.2 A;dI_G/dt = 0.2 A/μs				
		T2+ G+	50			A/μs
		T2+ G-	50			A/μs
		T2- G-	50			A/μs
		T2- G+	10			A/μs
Peak gate current	I_{GM}		2			A
Peak gate voltage	V_{GM}		5			V
Peak gate power	P_{GM}		5			W
Average gate power	$P_{G(AV)}$	over any 20 ms period	0.5			W
Storage temperature	T_{stg}		-40 to 150			℃
Operating junction temperature	T_j		125			℃
Thermal resistance junction to solder point	$R_{th\ j\text{-}sp}$	full or half cycle	15			K/W
Thermal resistance junction to ambient	$R_{th\ j\text{-}a}$	pcb mounted; minimum footprint	156			K/W
		pcb mounted;	70			K/W

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■ Electrical Characteristics Ta = 25℃

Parameter	Symbol	Testconditons	Min			Typ	Max			Unit
			··· E	··· F	··· G		··· E	··· F	··· G	
Gate trigger current	I_{GT}	V_D = 12 V; I_T = 0.1 A								
		T2+ G+				5	35	25	50	mA
		T2+ G-				8	35	25	50	mA
		T2- G-				11	35	25	50	mA
		T2- G+				30	70	70	100	mA
Latching current	I_L	V_D = 12 V; I_{GT} = 0.1 A								
		T2+ G+				7	20	20	30	mA
		T2+ G-				16	30	30	45	mA
		T2- G-				5	20	20	30	mA
		T2- G+				7	30	30	45	mA
Holding current	I_H	V_D = 12 V; I_{GT} = 0.1 A				5	15	15	30	mA
On-state voltage	V_T	I_T = 2 A				1.2		1.5		V
Gate trigger voltage	V_{GT}	V_D = 12 V; I_T = 0.1 A				0.7		1.5		V
		V_D = 400 V; I_T = 0.1 A		0.25		0.4				V
Off-state leakage current	I_D	V_D = $V_{DRM(max)}$;T_j = 125℃				0.1		0.5		mA
Critical rate of rise of off-state voltage	dV_D/dt	V_{DM} =67% $V_{DRM(max)}$;T_j = 125 ℃; exponential waveform; gate open circuit	100	50	200	250				V/μs
Critical rate of change of commutating voltage	dV_{com}/dt	V_{DM} = 400 V; T_j = 95 ℃; $I_{T(RMS)}$ = 1A;dI_{com}/dt = 1.8 A/ms; gate open circuit			10	50				V/μs
Gate controlled turn-on time	t_{gt}	I_{TM} = 1.5 A; V_D = $V_{DRM(max)}$;I_G = 0.1 A; dI_G/dt = 5 A/μs;				2				μs

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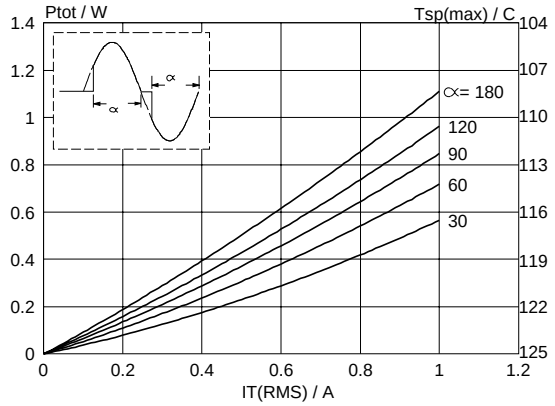

Fig.1. Maximum on-state dissipation, P_{tot}, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

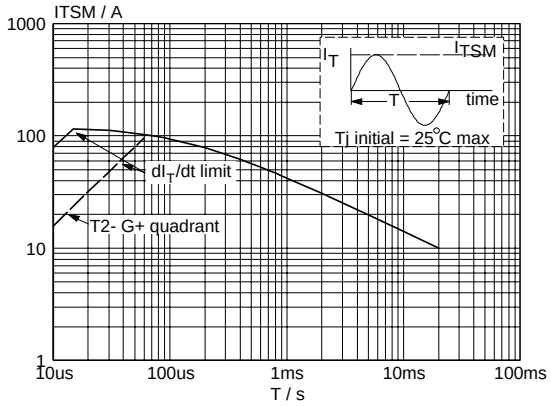

Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq 20ms$.

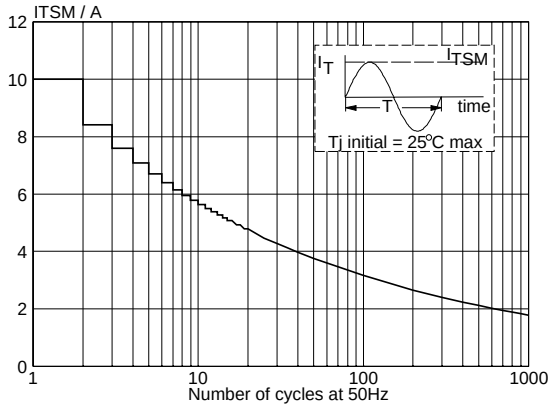

Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

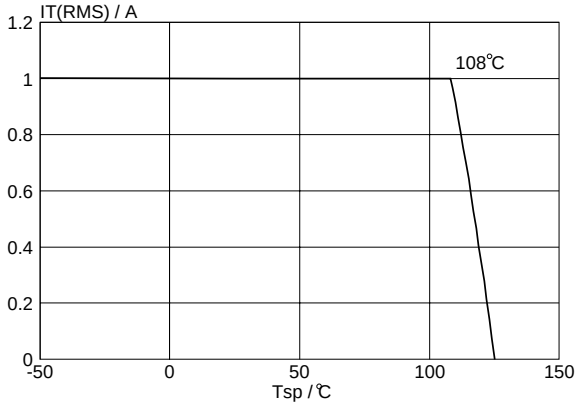

Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus solder point temperature T_{sp}.

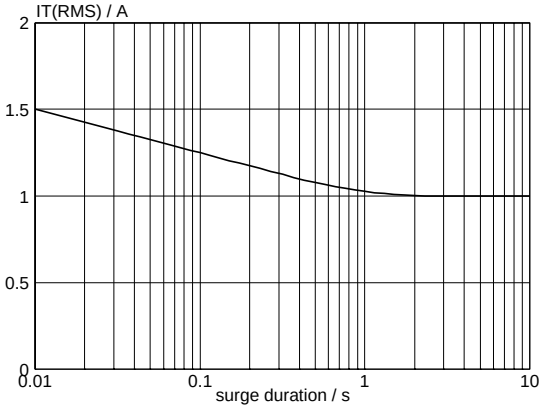

Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{sp} \leq 108^{\circ}C$.

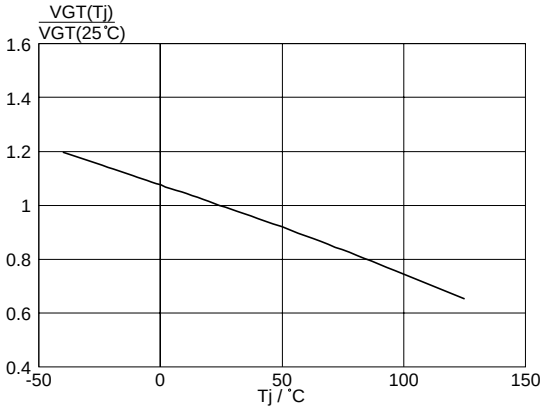

Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25^{\circ}C)$, versus junction temperature T_j.

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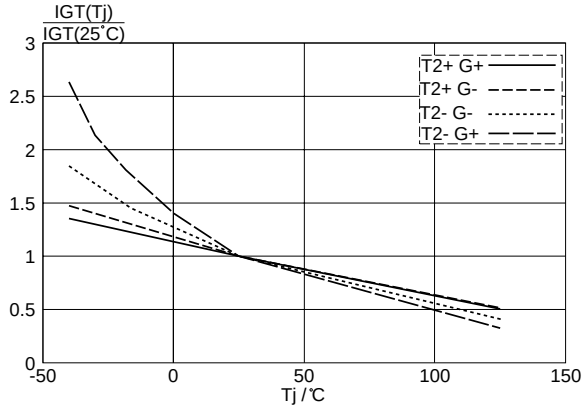

Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25^{\circ}C)$, versus junction temperature T_j.

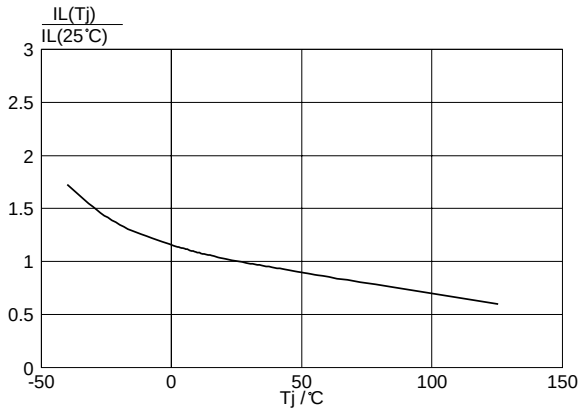

Fig.8. Normalised latching current $I_L(T_j)/ I_L(25^{\circ}C)$, versus junction temperature T_j.

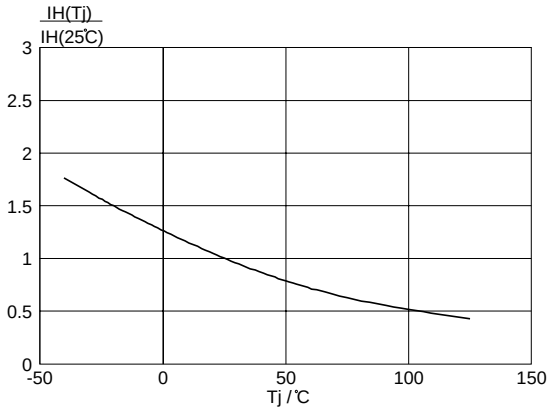

Fig.9. Normalised holding current $I_H(T_j)/ I_H(25^{\circ}C)$, versus junction temperature T_j.

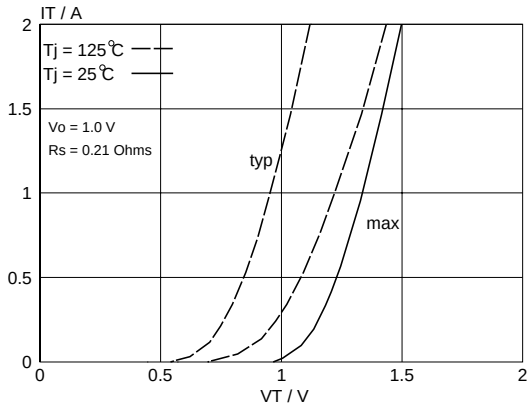

Fig.10. Typical and maximum on-state characteristic.

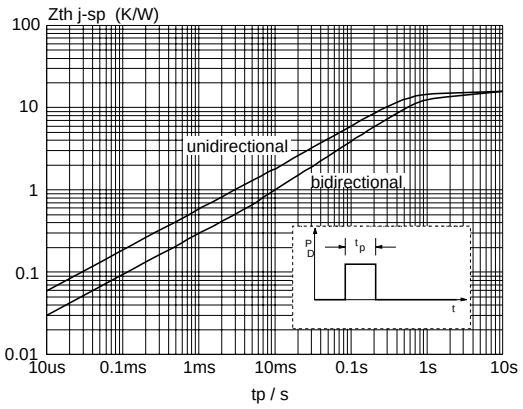

Fig.11. Transient thermal impedance $Z_{th\ j\text{-}sp}$, versus pulse width t_p.

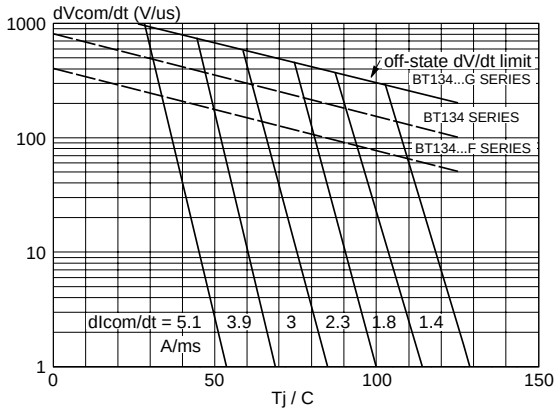

Fig.12. Typical commutation dV/dt versus junction temperature, parameter commutation dI_T should commutate when the dV/dt is below the value on the appropriate curve for pre-commutation dI_T/dt.